Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) In a system comprising an interconnect and a plurality of modules connected to said interconnect for putting packets of information onto the interconnect, wherein each packet comprises a number of fields containing information including both data and packet routing information, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data, a circuit comprising:

circuitry for receiving at least part of said information;

circuitry for determining if said at least part of said information satisfies one or more conditions; and

circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions wherein at least one of the one or more actions includes ; ~~and~~

~~means for~~ debugging the circuit by placing request/response packets on the interconnect for analysis.

2. (Original) A circuit as claimed in claim 1, wherein said action comprises the generation of a trace message.

3. (Original) A circuit as claimed in claim 1, wherein said action comprises the generation of an interrupt message.

4. (Original) A circuit as claimed in claim 3, wherein the interrupt is provided to one or more CPUs.

5. (Previously Presented) A circuit as claimed in claim 1, wherein said action is to prevent one or more modules from being granted access to the interconnect.

6. (Original) A circuit as claimed in claim 5, wherein circuitry is provided to prevent one or more modules from being granted access to the interconnect.

7. (Original) A circuit as claimed in claim 6, wherein said circuitry for preventing a module from putting further information onto the interconnect comprises a register.

8. (Original) A circuit as claimed in claim 7, wherein the register comprises one bit for each module and the value of said bit determines if the respective module is prevented from putting further information into the interconnect.

9. (Original) A circuit as claimed in claim 8, wherein at least one module is arranged to access said register non intrusively.

10. (Original) A circuit as claimed in claim 8, wherein a location is defined in said register for each module, the location being independent of the address of the module used by the interconnect.

11. (Original) A circuit as claimed in claim 1, wherein the module which puts the information onto the interconnect which matches the one or more conditions is prevented by the preventing circuitry from being granted access to the interconnect.

12. (Original) A circuit as claimed in claim 1, wherein the determining circuitry comprises comparator circuitry which compares the information on the interconnect with one or more match conditions.

13. (Original) A circuit as claimed in claim 1, wherein said conditions comprise one or more preconditions and one or more match conditions, said actions being performed when said one or more preconditions and said one or more match conditions have been satisfied.

14. (Original) A circuit as claimed in claim 13, wherein one precondition is that the one or more match conditions have occurred a predetermined number of times.

15. (Original) A circuit as claimed in claim 13, wherein one precondition is that the circuit is enabled.

16. (Original) A circuit as claimed in claim 13, wherein one precondition is that circuitry external to said circuit has been enabled.

17. (Original) A circuit as claimed in claim 16, wherein said external circuitry is a latch.

18. (Original) A circuit as claimed in claim 13, wherein said match conditions comprise one or more of the following:

an address or address range of the information;

the module or modules which put the information onto the interconnect;

the module or modules which are intended to receive the information on the interconnect; and

the type or types of transactions to which the information relates.

19. (Original) A circuit as claimed in claim 1, wherein storing circuitry is provided to store the information which satisfies the at least one condition.

20. (Cancelled).

21. (Previously Presented) A circuit as claimed in claim 1, wherein said packets of information comprises requests and responses.

22. (Currently Amended) A functional circuit comprising:

an interconnect;

one or more modules connected to the interconnect; and

a monitoring circuit for monitoring information containing packets put onto the interconnect by one or more modules, said information-containing packets including both data and packet routing information, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data, and said monitoring circuit comprising:

circuitry for determining if the information in a packet matches one or more conditions; and

circuitry for performing one or more actions if it is determined that information on the interconnect matches said one or more conditions wherein the one or more actions includes ; ~~and~~

~~means for~~ debugging the circuit by placing request/response packets on the interconnect for analysis.

23. (Previously Presented) A functional circuit as claimed in claim 22, wherein the functional circuit is an integrated circuit.

24. (Previously Presented) A functional circuit as claimed in claim 23, wherein at least one module is external to said integrated circuit.

25. (Previously Presented) A functional circuit as claimed in claim 22, wherein an arbiter is provided for arbitrating between the modules to determine which module is granted access to the interconnect at a given time.

26. (Previously Presented) A functional circuit as claimed in claim 25, wherein said determining circuitry is at least partially in the arbiter.

27. (Previously Presented) A functional circuit as claimed in claim 25, wherein said determining circuit does not delay the arbitration provided by the arbiter.

28. (Previously Presented) A functional circuit as claimed in claim 22, wherein said interconnect is a bus.

29. (Previously Presented) A functional circuit as claimed in claim 22, wherein one of said modules comprises a debug module.

30. (Previously Presented) A functional circuit as claimed in claim 29, wherein at least some of said circuitry for performing at least one action is in said debug module.

31. (Previously Presented) A functional circuit as claimed in claim 25, wherein at least some of said circuitry for performing at least one action is in said arbiter.

32. (Previously Presented) A functional circuit as claimed in claim 29, wherein at least part of the determining circuitry is in the debug module.

33. (Previously Presented) A method comprising the steps of:

monitoring information containing packets on an interconnect, the information being put onto the interconnect by one or more modules, said information-containing

packets including both data and packet routing information, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data;

determining if the information on an interconnect satisfies one or more conditions;

carrying out one or more actions if it is determined that the information containing packet satisfies one or more conditions; and

debugging the circuit by placing request/response packets on the interconnect for analysis.

34. (Previously Presented) A circuit for monitoring packets of information on an interconnect, said packets of information being put onto the interconnect by one or more modules connected to the interconnect, wherein said packets of information include both data and packet routing information, and wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data, said circuit being arranged to determine if the information satisfies one or more conditions, the circuit including means for debugging the circuit by placing request/response packets on the interconnect for analysis.

35. (Previously Presented) A circuit for monitoring packets of information on an interconnect, said packets of information including both data and packet routing information and said packets of information being put onto the interconnect by one or more modules connected to the interconnect, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data, and wherein said circuit being arranged to determine if the information satisfies one or more conditions and to select the information satisfying the one or more conditions, the circuit

including means for debugging the circuit by placing request/response packets on the interconnect for analysis.

36. (Currently Amended) A circuit in a system comprising an interconnect and a plurality of modules connected to said interconnect for putting packet-format information onto the interconnect, wherein each packet comprises a number of fields containing information, including a routing field, an address field, a source field, a transaction type field, a transaction identifier field, and an operation code field, and wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules, the circuit comprising:

circuitry for receiving at least part of said information from at least one of said fields;

circuitry for determining if said at least part of said information satisfies one or more conditions; and

circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions wherein the one or more actions includes ; ~~and~~

~~means for~~ debugging the circuit ~~by placing request/response packets~~ on the interconnect ~~for analysis~~.